Yaohua Zhang

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Education

2016 – 2020 **MEng Electrical and Electronic Engineering, Imperial College London**
First Class Honours

2010 – 2015 **Raffles Institution, Singapore**

- SINGAPORE-CAMBRIDGE GCE A Levels: Chemistry (A), Physics (A), Mathematics (A), Economics (A), Project Work (A), General Paper (A) [Perfect University Admissions Score]

Employment

Apr – Aug 2019 **Embedded System Engineer Intern, DnaNudge Ltd**

- Designed a power management adaptor board using Altium Designer from scratch and worked with the supply chain manager to liaise with PCB manufacturers to ensure prompt delivery.
- Developed an entire I^2C device library for ICM-20648 (motion sensor unit) and nRF52832 (microcontroller) to aid future firmware R&D. Proficient in embedded system development, Nordic SDK, Arm Keil MDK.
- In charge of product (DnaBand) usability testing and design verification, authored extensive product test procedures and other relevant technical files. Gained insight into compliance testing, CE marking, and IP code.
- Designed a 4-layer evaluation board (150+ components, 400+ connections) in Altium Designer to aid future hardware (DnaBand) R&D.

Jan – Mar 2019 **Teaching Assistant, EE Department, Imperial College London**

- EE1&EE2 Mathematics

Conducted weekly Q&A sessions for first and second year students. Explained more difficult concepts like Fourier analysis, multivariable calculus, and linear algebra in greater detail to students.

- EE2-04 Communication Systems Lab Instructor

Assisted students in learning LabVIEW and communication concepts like amplitude and frequency modulation, z-transform, information theory and coding theory.

Jul - Aug 2018 **Research Intern, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore**

- Supervised by Prof Y. P. Zhang. Successfully completed a project to investigate antenna performance and analyse the differential integrated antenna. Wrote a MATLAB script which analysed the performance of singled-ended vs differential patch antennas as well as a technical report that explored the quality factor of radiating structures.
- Developed proficiency with MATLAB for analytic modelling of antenna performance.

Jul - Aug 2017 **Research Intern, Undergraduate Research Opportunity Program (UROP) Imperial College London**

- Supervised by Prof A. Manikas. Received the prestigious Imperial College British Petroleum Award (£1600) to fund my UROP.
- Successfully completed an 8-week project on Software Defined Radio and its applications using USRP hardware and LabVIEW.
- Coded a real-time communication system that can transceive text messages using Quadrature Phase Shift Keying (QPSK).
- Developed proficiency with LabVIEW and acquired experience of applying mathematical techniques for use in signal processing.

Technical Projects

Oct 2019 – Jun 2020 Optimal Design of Integrated Circuits for the Body Dust Project

- Final Year Project that runs throughout the academic year. Supervised by Dr Pantelis Georgiou and Dr Sandro Carrara (EPFL).
- Analysed existing potentiostat topologies and simulated them in Cadence Spectre with TSMC 180 nm technology. Identified potential areas for optimisation.
- Designed optimised potentiostat circuits using the g_m/I_D methodology and pre-computed lookup tables, with emphasis on low power, small area, and high SNR.
- Constructed a novel figure of merit (a weighted Euclidean distance) to assess circuit performance.
- Successfully extended the g_m/I_D methodology into the design of low power circuits. In most of the existing work, the g_m/I_D methodology is being used to design high performance analogue circuits that are not necessarily optimised for low power dissipation.
- An IEEE ISCAS 2021 paper is currently in preparation with the supervisors mentioned above as co-authors.

Oct – Dec 2019 Full Custom Design of a 10-bit ADC in 180 nm CMOS

- This project was part of the coursework requirements for the EE4-20 Full Custom IC Design module.
- Designed a 10-bit successive approximation ADC based on binary weighted capacitors to optimise for resolution and meet other technical specifications like power, size, and speed. Completed schematic design, circuit simulation of ADC in Cadence GPDK 180 nm.
- The ADC consists of 4 sub-systems: a high precision voltage reference, a DAC with inherent sample-and-hold function, a high-resolution comparator, and the digital circuitry to control the conversion process and to stream out the corresponding digital code.
- Wrote an IEEE-style paper detailing the ADC system overview, circuit implementation, simulated results, and limitations of design.

Jan – Mar 2019 Submicron FET Simulation and Optimisation

- This project was completed as part of the requirements for the EE3-11 Advanced Electronic Devices module.
- Investigated the impact of short channel effects on MOSFET performance by simulating a MOSFET with 150nm gate length in Sentaurus.
- Optimised MOSFET performance through a combination of techniques like thinning oxide layer, increasing substrate doping and reducing junction depth.
- Used Sentaurus Device Editor to implement a GAA FET (Gate-all-around field effect transistor).
- Wrote an IEEE-style paper to investigate how cross-sectional geometry can affect its performance. Used DC performance characteristics like sub-threshold swing, drain-induced barrier lowering, output conductance, on-off current ratio to judge the FET's performance.

Jan – Mar 2019 Complex Impedance Meter

- This project was completed as part of the requirements for the EE3-01 Instrumentation module.
- Designed a complex impedance measurement instrument that could measure impedance magnitude of 100 Ω to 100 kΩ and phase from -180 to 180 degrees accurately up to 100 kHz.
- Gained proficiency in PCB design using Altium CircuitMaker. Soldered all components (surface mount and through-hole) onto the 2-layer PCB bare board.
- Wrote microcontroller (NXP LPC1768) code (C++) in Arm mbed to control frequencies, amplitudes and gains as well as to conduct signal processing with a moving average filter.